High Speed, RRIO, Push-Pull Output Comparator

1 FEATURES

- **High Speed, 40ns Propagation Delay**
- **Low Supply Current: 120μA(TYP) at V_{CC}=5V**
- **Rail-to-Rail Input and Output**
- **Push-Pull Outputs**
- **Supply Range: +2.7V to +5.5V**
- **-40°C to +125°C Operating Temperature**
- **Micro Size Packages: SOT23-5, SC70-5**

2 APPLICATIONS

- **Overvoltage and Undervoltage Detection**
- **Multivibrators**
- **Overcurrent Detection**
- **Line Receivers**
- **System Monitoring**
- **Battery-Powered Systems**
- **Sampling Circuits**

3 DESCRIPTIONS

The RES3021 of fers a w i d e s u p p l y vol t agerang e, lo w quiescent current 120μA(Typical), high speed and rail-to-rail inputs. All these features come in industry-standard and extremely small packages, making this device an excellent choice for low-voltage and low-power applications for portable electronics and industrial systems.

Featuring a push-pull output stage, the RES3021 a l lo w s for operation with absolute minimum power consumption when driving any capacitive or resistive load.

The devices are ideal for system monitoring, include tablets, portable medical, s m a r t p h on es.The RES3021 is specified at the full temperature range of −40°C to +125°C under single power supplies of 2.7V to 5.5V.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RES3021IUR	SOT23-5	1.60mm×2.92mm
RES3021IDR	SC70-5	2.10mm×1.25mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

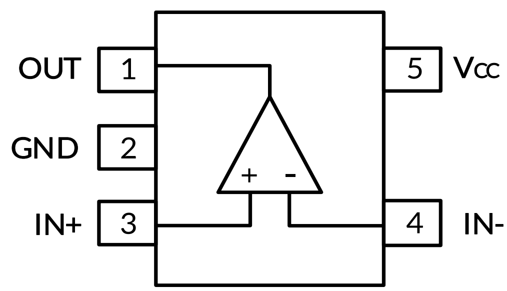
5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RES3021	RES3021IUR	-40°C ~125°C	SOT23-5	RES3021IUR	MSL3	Tape and Reel, 3000
	RES3021IDR	-40°C ~125°C	SC70-5 (4)	RES3021IDR	MSL3	Tape and Reel, 3000

NOTE:
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
(2) There may be additional marking, which relates to the lot trace code information(data code and vendor code), the logo or the environmental category on the device.
(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.
(4) Equivalent to SOT353.

6 Pin Configuration and Functions (Top View)

RES3021IUR,RES3021IDR



SOT23-5/SC70-5

Pin Description

NAME	RES3021IUR,RES3021IDR SOT23-5/SC70-5	I/O (1)	DESCRIPTION
OUT	1	O	Output
GND	2	-	Ground.
IN+	3	I	Positive input
IN-	4	I	Negative input
V_{CC}	5	P	Positive (highest) power supply

(1) I=Input, O=Output, P=Power.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	Supply voltage			7	V
	Input pin (IN+, IN-) (2)		-0.3	(V_{CC}) +0.3	
	Signal output pin (3)		-0.3	(V_{CC}) +0.3	
Current	Signal input pin (IN+, IN-) (2)		-10	10	mA
	Signal output pin (3)		-100	100	mA
	Output short-circuit (4)		Continuous		mA
θ_{JA}	Package thermal impedance (5)	SOT23-5		230	°C/W
		SC70-5		380	
Temperature	Operating range, T_A		-40	125	°C
	Junction, T_J (6)		-40	150	
	Storage, T_{stg}		-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3V beyond the supply rails should be current-limited to ±100mA or less.
(4) Short-circuit to ground, one amplifier per package.
(5) The package thermal impedance is calculated in accordance with JESD-51.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Machine Model (MM)	±450	
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, Vs= (V+) - (V-)	Single-supply	2.7		5.5	V
	Dual-supply	±1.35		±2.75	

7.4 ELECTRICAL CHARACTERISTICS: V_{CC}=2.7V

(At T_A = +25°C, V_{CC}=2.7V, unless otherwise noted.) (1)

PARAMETER		CONDITIONS	RES3021IDR,RES3021IUR			UNIT
			MIN(2)	TYP(3)	MAX(2)	
POWER SUPPLY						
V_{CC}	Operating Voltage Range		2.7		5.5	V
I_Q	Quiescent Current	T_A = 25°C		117		µA
PSRR	Power-Supply Rejection Ratio	V_S=2.7V to 5.5V, V_{CM}=V_{CC}/2	60	75		dB
INPUT						
Vos	Input Offset Voltage	V_{CM} =V_{CC}/2	-20	±3	20	mV
ΔVos/ΔT	Input Offset Voltage Drift	T_A = –40°C to 125°C		±2		µV/°C
	Input Hysteresis			1		mV
IB	Input Bias Current (4) (5)	V_{CM} =V_{CC}/2		1	100	pA
V_{CM}	Common-Mode Voltage Range	T_A = –40°C to 125°C	(V-)-0.1		(V+)+0.1	V
CMRR	Common-Mode Rejection Ratio	V_{CM} =-0.1V to 2.8V	60	75		dB
OUTPUT						
V_{OH}	Output Swing From Upper Rail	I_{SOURCE} = 4mA		255		mV
V_{OL}	Output Swing From Lower Rail	I_{SINK} = 4mA		230		mV
I_{SC}	Short Circuit Sink Current	I_{SC} sinking		13		mA
	Short Circuit Source Current	I_{SC} sourcing		14		mA
SWITCHING						
T_{PHL}	Propagation Delay H To L (6)	Overdrive = 100 mV, C_L = 15pF		30		ns
T_{PLH}	Propagation Delay L To H (6)	Overdrive = 100 mV, C_L = 15pF		32		
T_R	Rise Time	10% to 90%		2		ns
T_F	Fall Time	10% to 90%		2		ns

NOTE:
(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(4) This parameter is ensured by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.
(6) High-to-low and low-to-high refers to the transition at the input.

7.5 ELECTRICAL CHARACTERISTICS: V_{CC}=5V

(At T_A = +25°C, V_{CC}=5V, unless otherwise noted.) (1)

PARAMETER		CONDITIONS	RES3021IDR,RES3021IUR			UNIT
			MIN(2)	TYP(3)	MAX(2)	
POWER SUPPLY						
V_S	Operating Voltage Range		2.7		5.5	V
I_Q	Quiescent Current	T_A = 25°C		120	225	µA
PSRR	Power-Supply Rejection Ratio	V_S=2.7V to 5.5V, V_{CM}=V_{CC}/2	60	75		dB
INPUT						
Vos	Input Offset Voltage	V_{CM}=V_{CC}/2	-20	±3	20	mV
ΔVos/ΔT	Input Offset Voltage Drift	T_A = –40°C to 125°C		±2		µV/°C
	Input Hysteresis			1		mV
IB	Input Bias Current (4) (5)	V_{CM}=V_{CC}/2		1	100	pA
V_{CM}	Common-Mode Voltage Range	T_A = –40°C to 125°C	(V-)-0.1		(V+)+0.1	V
CMRR	Common-Mode Rejection Ratio	V_{CM} =-0.1V to 5.1V	60	75		dB
OUTPUT						
V_{OH}	Output Swing From Upper Rail	I_{SOURCE} = 4mA		150		mV
V_{OL}	Output Swing From Lower Rail	I_{SINK} = 4mA		160		mV
I_{SC}	Short Circuit Sink Current	I_{SC} sinking	30	40		mA
	Short Circuit Source Current	I_{SC} sourcing	36	46		mA
SWITCHING						
T_{PHL}	Propagation Delay H To L (6)	Overdrive = 100 mV, C_L = 15pF		25		ns
T_{PLH}	Propagation Delay L To H (6)	Overdrive = 100 mV, C_L = 15pF		30		
T_R	Rise Time	10% to 90%		2		ns
T_F	Fall Time	10% to 90%		2		ns

NOTE:
(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(4) This parameter is ensured by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.
(6) High-to-low and low-to-high refers to the transition at the input.

7.6 Timing Diagrams

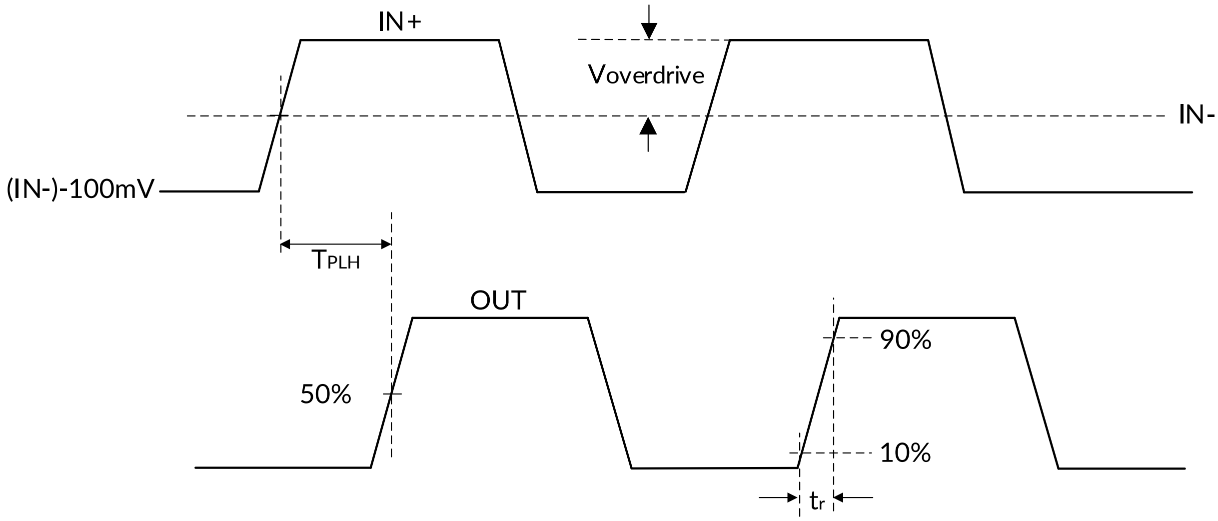


Figure 1. T_{PLH} Timing Diagram

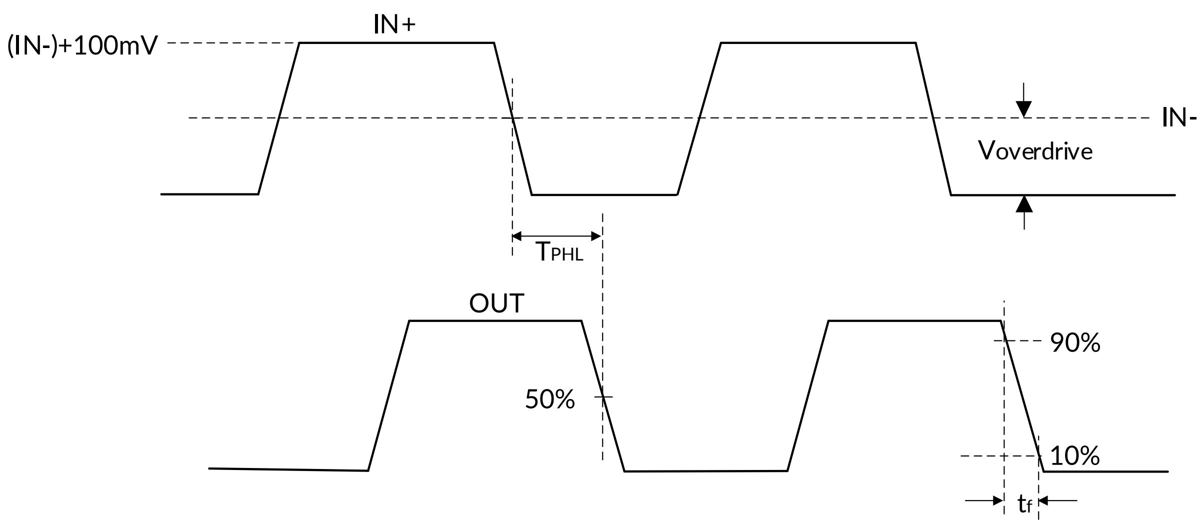


Figure 2. T_{PHL} Timing Diagram

7.7 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A = +25°C, V_{CC}=5V, unless otherwise noted.

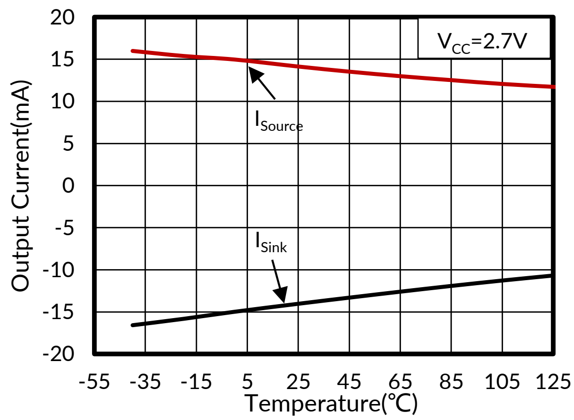


Figure 3. Output Current vs Temperature

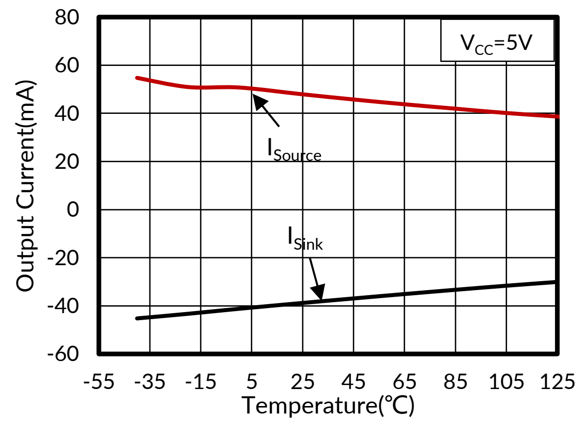


Figure 4. Output Current vs Temperature

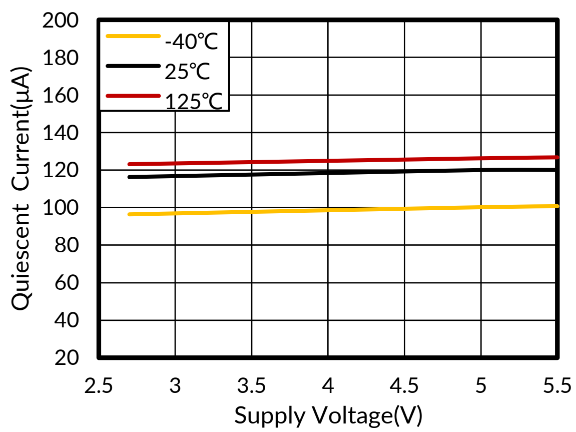


Figure 5. Quiescent Current vs Supply Voltage

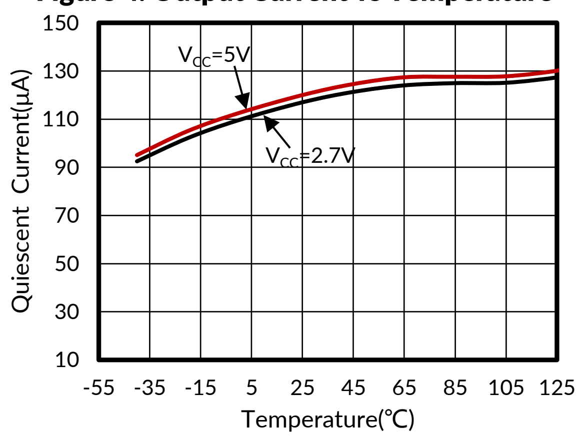


Figure 6. Quiescent Current vs Temperature

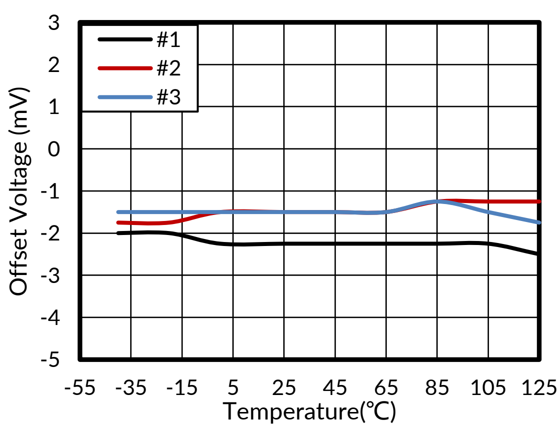


Figure 7. Offset Voltage vs Temperature

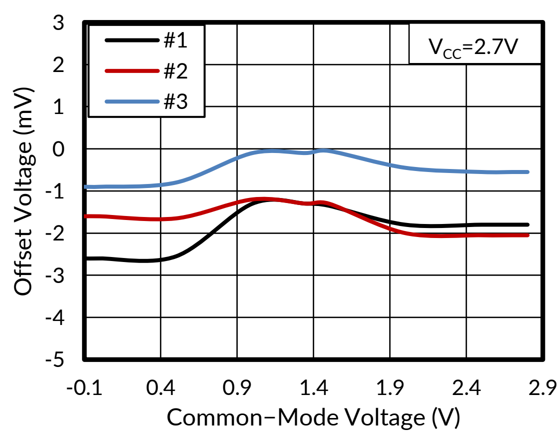


Figure 8. Offset Voltage vs Common-Mode Voltage

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A = +25°C, V_{CC}=5V, unless otherwise noted.

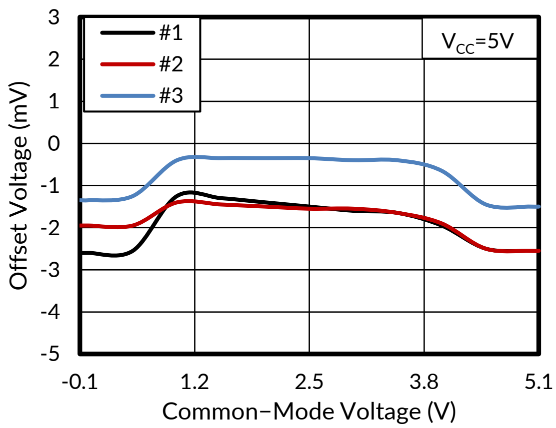


Figure 9. Offset Voltage vs Common-Mode Voltage

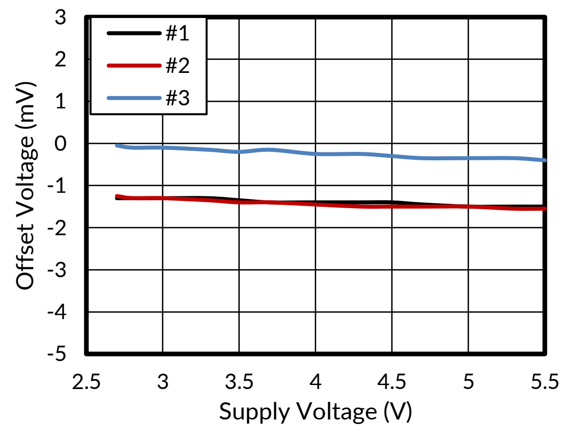


Figure 10. Offset Voltage vs Power Supply

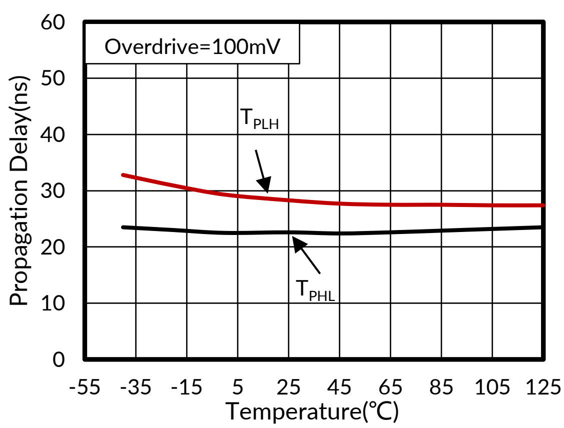


Figure 11. Propagation Delay vs Temperature

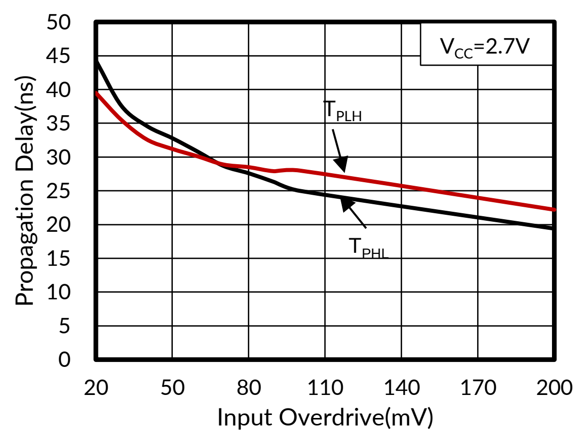


Figure 12. Propagation Delay vs Input Overdrive

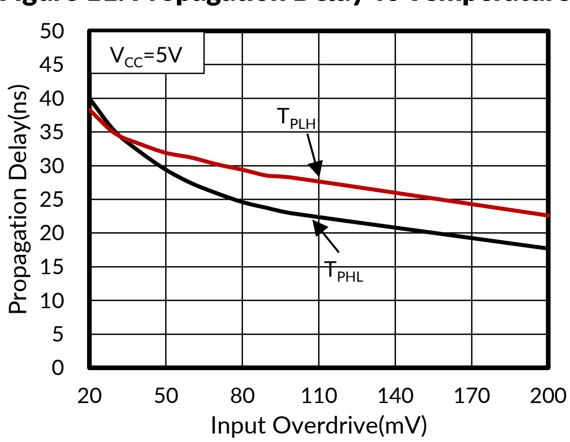


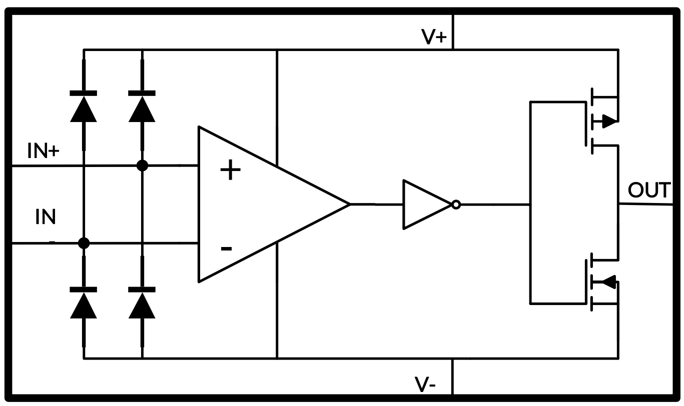
Figure 13. Propagation Delay vs Input Overdrive

8 Detailed Description

8.1 Overview

The RES3021 devices single-channel, low-power, high speed comparator with a push-pull output stage. Operating from 2.7V to 5.5V and consuming only 120μA. The push-pull output of the RES3021 supports rail to rail output swing and interfaces with TTL/CMOS logic. The RES3021 devices feature 40ns response time, and include 1 mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.1 V beyond the power-supply rails.

8.2 Functional Block Diagram



8.3 Feature Description

The RES3021 device is low-power comparator that can operate at low voltage. The RES3021 features a rail-to-rail input stage capable of operating up to 100 mV beyond the V_{CC} power supply rail.

8.4 Input Stage

The RES3021 has rail-to-rail input common-mode voltage range. It can operate at any differential input voltage within this limit as long as the differential voltage is greater than zero. A differential input of zero volts may result in oscillation.

The differential input stage of the comparator is a pair of PMOS and NMOS transistors, therefore, no current flows into the device. The input bias current measured is the leakage current in the MOS transistors and input protection diodes. This low bias current allows the comparator to interface with a variety of circuitry and devices with minimal concern about matching the input resistances.

8.5 Output Stage

The RES3021 has a CMOS push-pull rail-to-rail output stage. The push-pull transistor configuration of the output keeps the total system power consumption to a minimum. No power is wasted through the pull-up resistor when the output is low. The output stage is specifically designed with dead time between the time when one transistor is turned off and the other is turned on (break-before-make) to minimize shoot through currents. The internal logic controls the break-before-make timing of the output transistors. The break-before-make delay varies with temperature and power condition.

8.6 Output Current

The output can drive very large current. The RES3021 can source up to 46mA and can sink up to 40mA, when operated at 5V supply. This large current handling capability allows driving heavy loads directly.

9 Application Information

9.1 External Hysteresis

The RES3021 have a hysteresis transfer curve (shown in Figure 14) that is a function of three components: V_{TH}, V_{OS}, and V_{HYST}.

- V_{TH}: the actual set voltage or threshold trip voltage
- V_{OS}: the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST}: internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

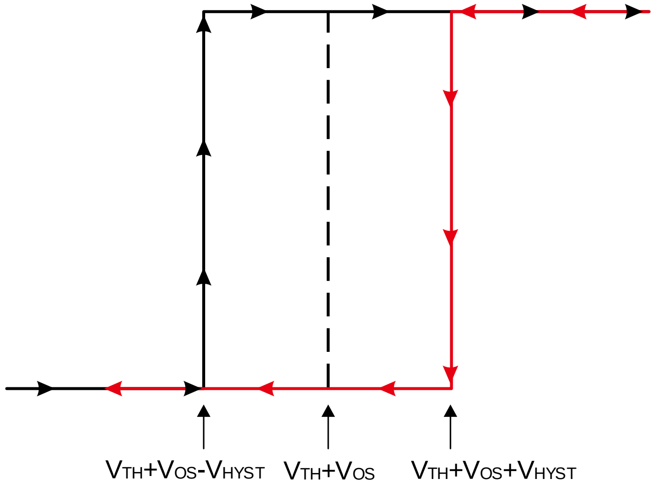


Figure 14. RES3021 Hysteresis Transfer Curve

9.2 Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 15. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. The lower input trip voltage (V_{A1}) is defined by Equation 1:

$$V_{A1} = V_{CC} \times \frac{R2}{(R1||R3)+R2} \quad (1)$$

When V_{IN} is greater than [V_A × (V_{IN} > V_A)], the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. The upper trip voltage (V_{A2}) is defined by Equation 2:

$$V_{A2} = V_{CC} \times \frac{R2||R3}{(R2||R3)+R1} \quad (2)$$

The total hysteresis provided by the network is defined by Equation 3:

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

Application Information(continued)

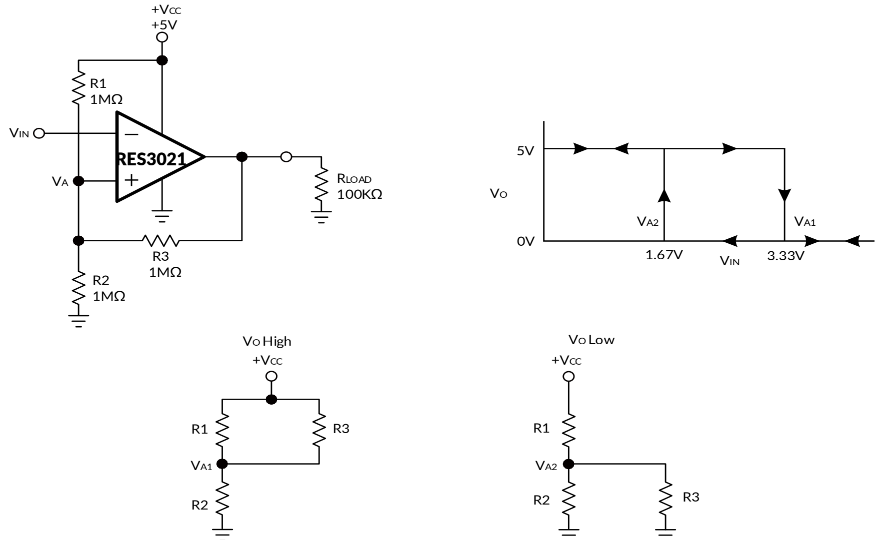


Figure 15. RES3021 in Inverting Configuration With Hysteresis

9.3 Noninverting Comparator with Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure16, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1}. V_{IN1} is calculated by Equation 4：

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} \times V_{REF} \quad (4)$$

When V_{IN} is high, the output is also high. For the comparator to switch back to a low state, V_{IN} must equal V_{REF} before V_A is again equal to V_{REF}. V_{IN} can be calculated by Equation 5：

$$V_{IN2} = \frac{V_{REF}(R1+R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between VIN1 and VIN2, as defined by Equation 6：

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

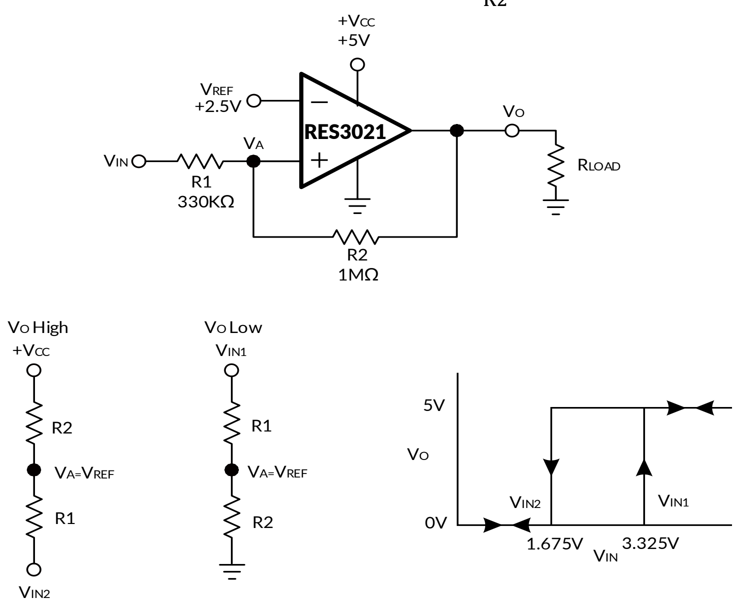


Figure 16. RES3021 in NoninvertingConf g urat ion wi thHyste r esis

10 Layout

10.1 Layout Guidelines

The RES3021 are fast-switching, high-speed comparators and require high-speed layout considerations. For best results, maintain the following layout guidelines.

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane.
- Place decoupling capacitors (0.1μF and 1μF ceramic, surface-mount capacitor) as close as possible to V_{CC}. Using multiple bypass capacitors in different decade ranges such as 10pF, 1nF, 100nF and 1μF provides the best noise reduction across frequency ranges.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane runs between the output and inputs.
- The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

10.2 Layout Example

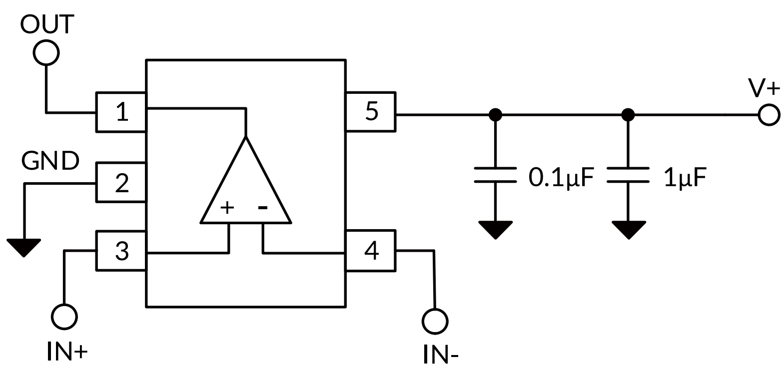
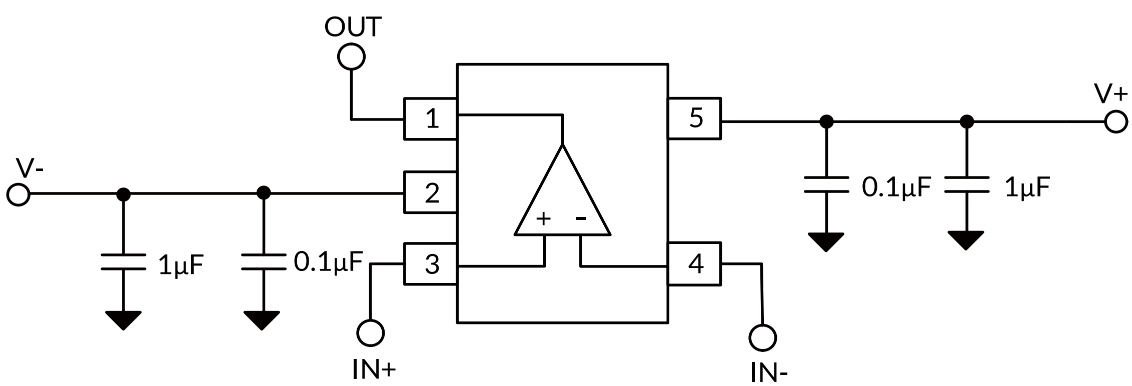


Figure 17. RES3201 Singlesupply Layout Example

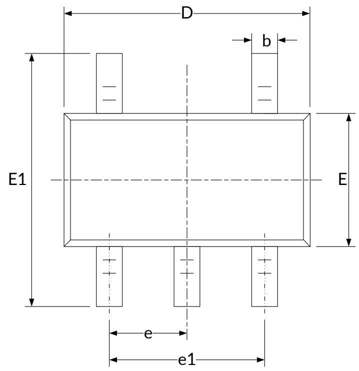


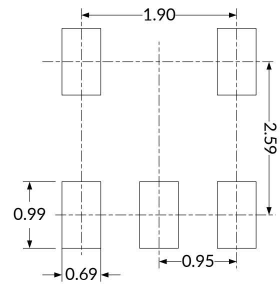
NOTE: If dual power supply is used, it is necessary to place decoupling capacitors (0.1μF and 1uF ceramic, surface-mount capacitor) as close as possible to V+ and V-.

Figure 18RES3021 dual-supply Layout Example

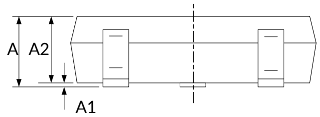
11 PACKAGE OUTLINE DIMENSIONS

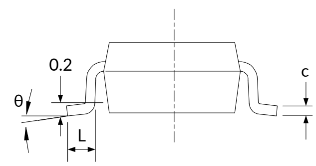
SOT23-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



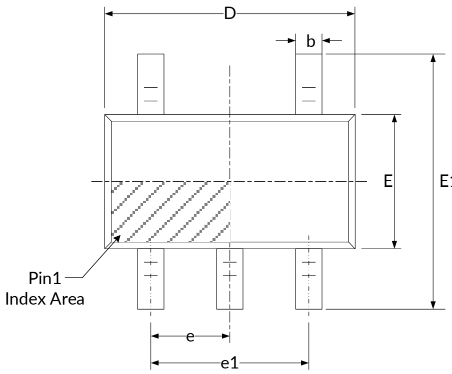


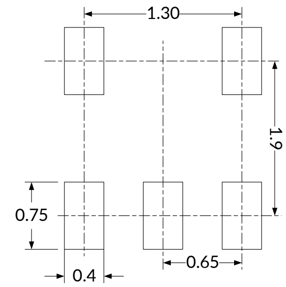
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

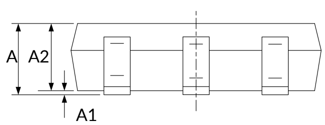
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

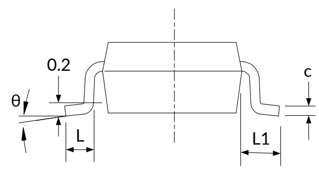
SC70-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



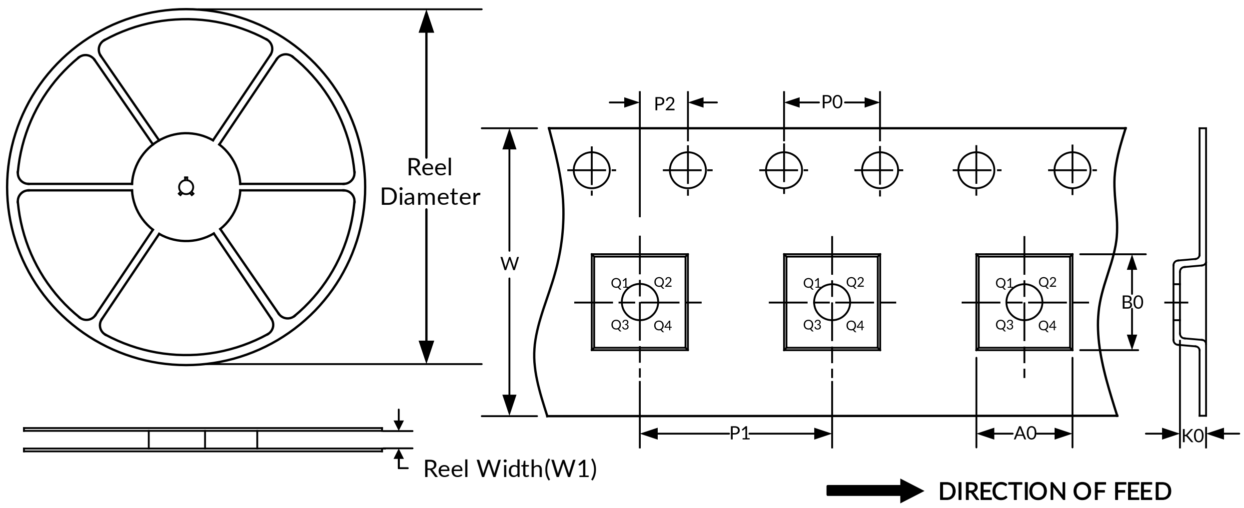


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D (1)	2.000	2.200	0.079	0.087
E (1)	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC) (2)		0.026(BSC) (2)	
e1	1.300(BSC) (2)		0.051(BSC) (2)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°

NOTE:
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS **TAPE DIMENSION**



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7”	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SC70-5	7”	9.5	2.25	2.55	1.20	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.